



# Thermal Aware On-Die Electrical Analysis

## Authors:-

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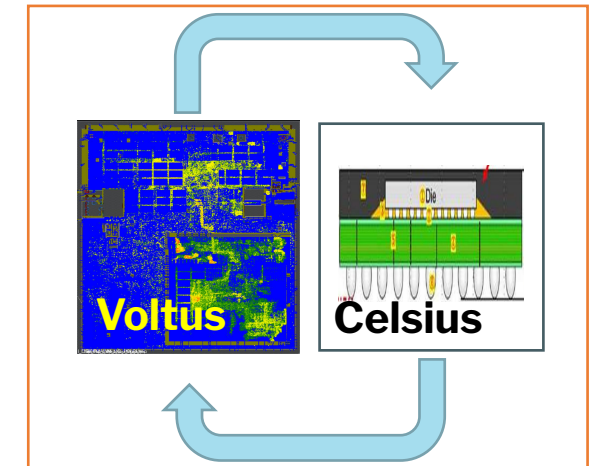
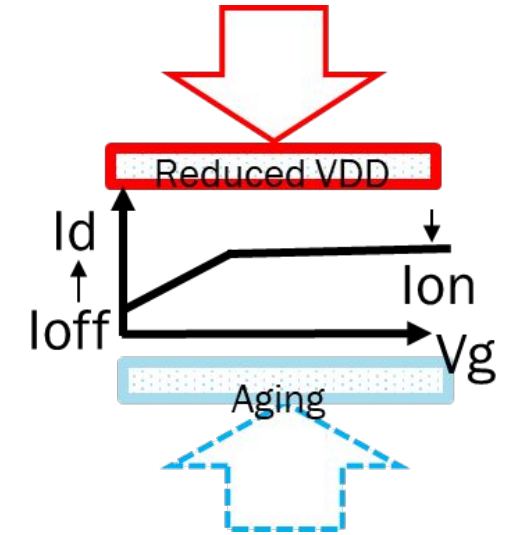
# Agenda

- Motivation
- Chip Design Challenges
- Thermal Aware Solution
- Thermal Analysis Results
- Conclusion
- Acknowledgements



# Motivation

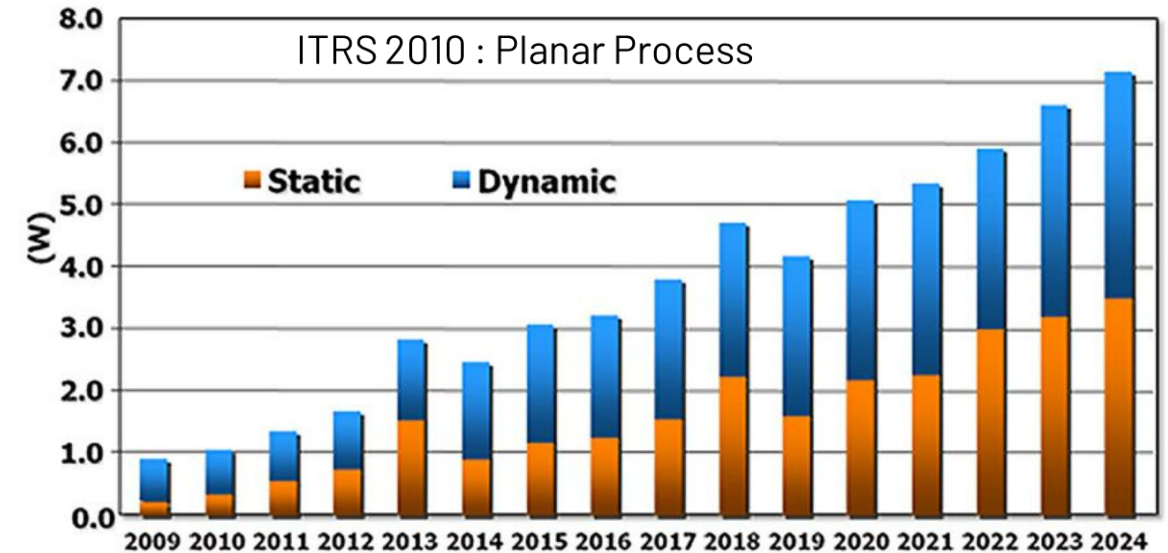
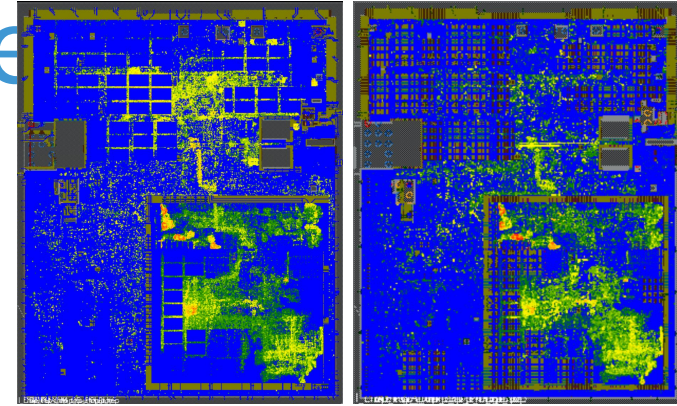
- Existing solutions not adequate for modern-day high-power chips for hotspots
- Designs are getting bigger, leads to higher power dissipation and reliability issues (Electro-migration/EM, aging effects)
- Chip level thermal analysis alone is not sufficient for a complex system (Chip + Package + Board)
- Closed loop Electro-Thermal analysis for overall system is necessary for today's designs
- Early and accurate system level thermal analysis is essential





# Design for Thermal Challenge

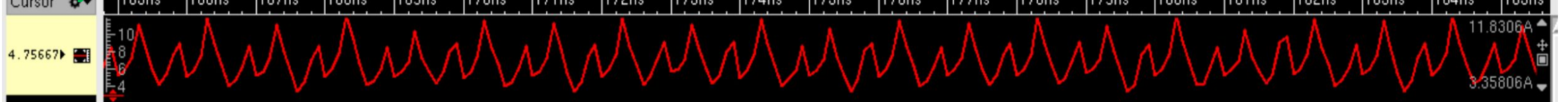
- Area increase contributes to  $T_j$ 
  - Chip size may not scale linearly with process node
  - Larger Heat Source due to increased Junction temperature
- Power and Performance: ( $T_j + \Delta T_j$ )
  - Higher Power Density
- SiP: More than Moore integration
  - Multi-Die in different process nodes



Static/Leakage Power Density: Area

Dynamic Power Density: Area +

Activity



# Thermal Aware Design at Chip & System Level

## ○ Chip Level

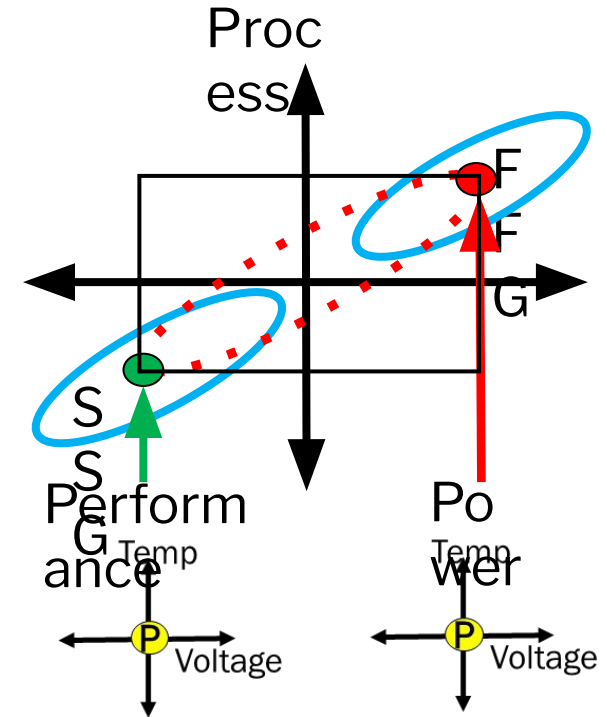
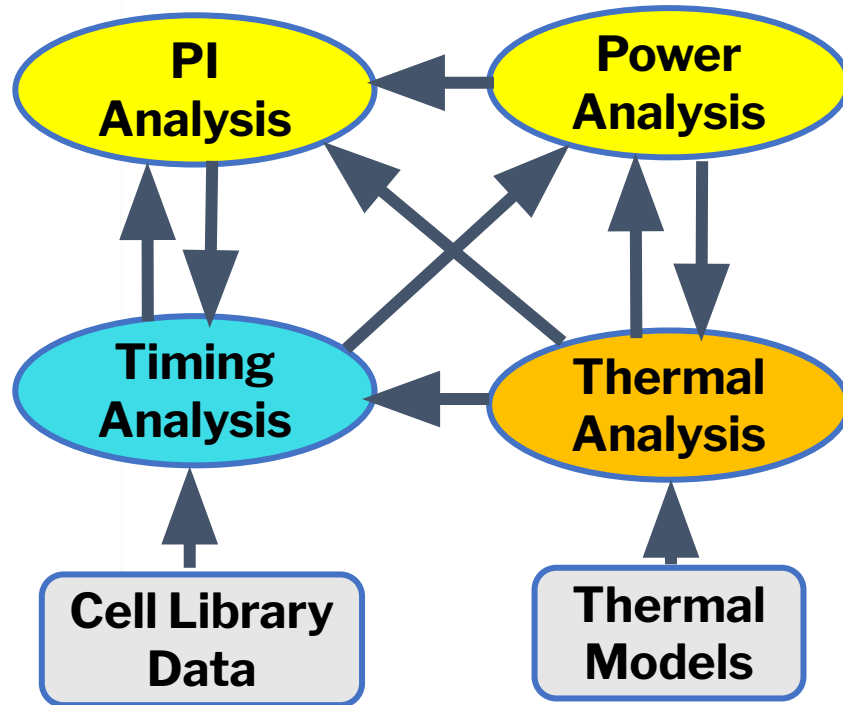
- Pessimism removal in timing sign-off due to depth based derate approach for timing sign-off
- Metal and Device self-heating impact on SOC aging/lifetime, reliability
- Power and signal integrity signoff based on system aware on-chip temperature gradient.

## ○ System Level

- System aware component level temperature map being a function of on-field test cases would enable effective system level thermal solutions
- System aware Chip+Package level thermal map closely follows the ambient temperature cycle, and application specific test on field. This helps customer to have application specific thermal solutions



# Electro-Thermal Analysis



- Process Variation
  - Multiple Lib corner sign-off
- Global Junction Temperature
  - Temperature variation : Application specific
- Power Supply Noise/Ripple Margin
  - Depth based de-rate with Max 5% ripple target

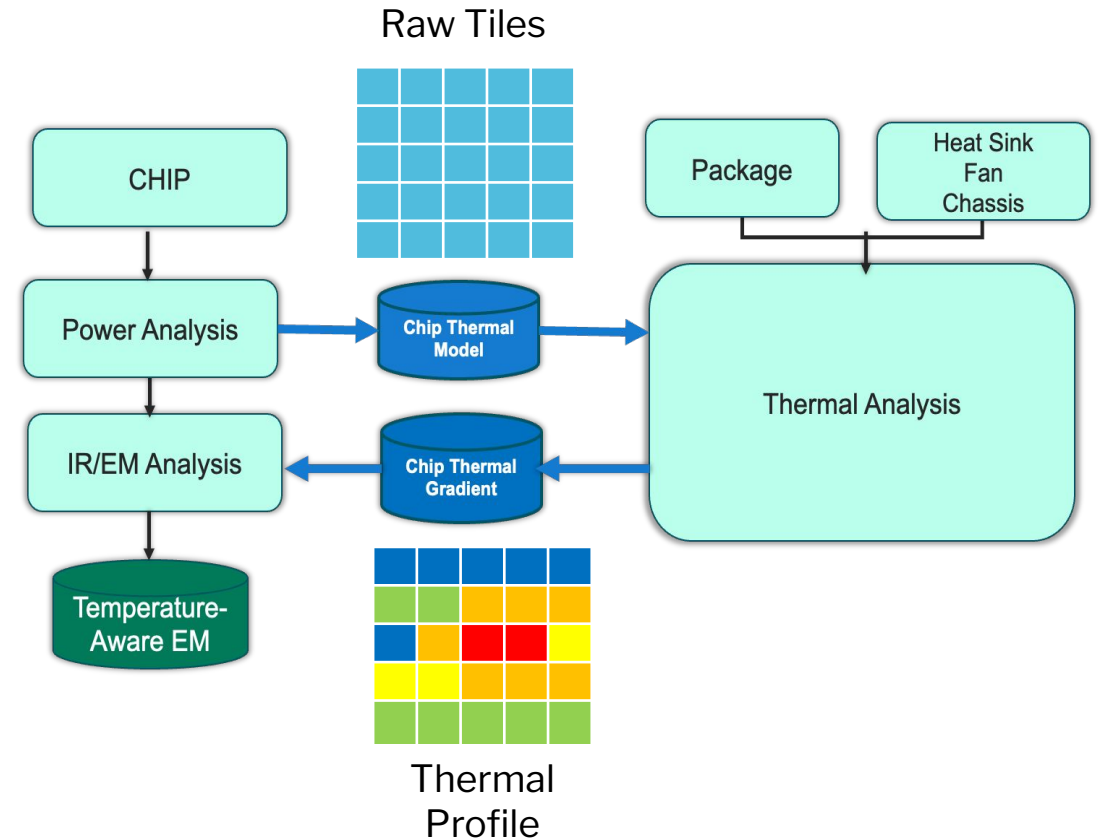


# Proposed solution: Thermal aware electrical analysis



# Thermal Aware Electrical Analysis Solution

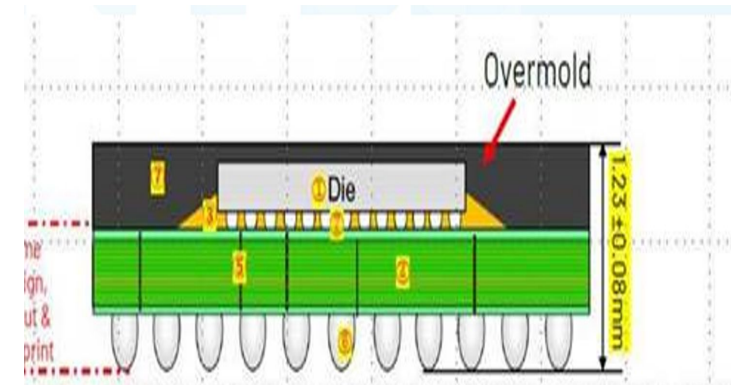
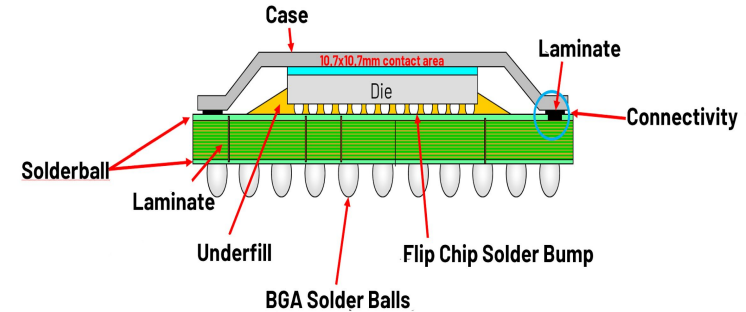
- Adequate thermal margin for System level analysis
  - Signal Integrity (SI), Power Integrity(PI), and Thermal Sign-off
- Chip Thermal Model generation
  - Tile based Power distribution of the Chip fed to Thermal analysis tool
- On Chip Temperature Gradient
  - Chip+Package+Board thermal profile generated
- Thermal aware PI analysis ( DC-IR and EM)
  - Use Thermal profile for electrical analysis





# Thermal Analysis Setup: Tool, Models

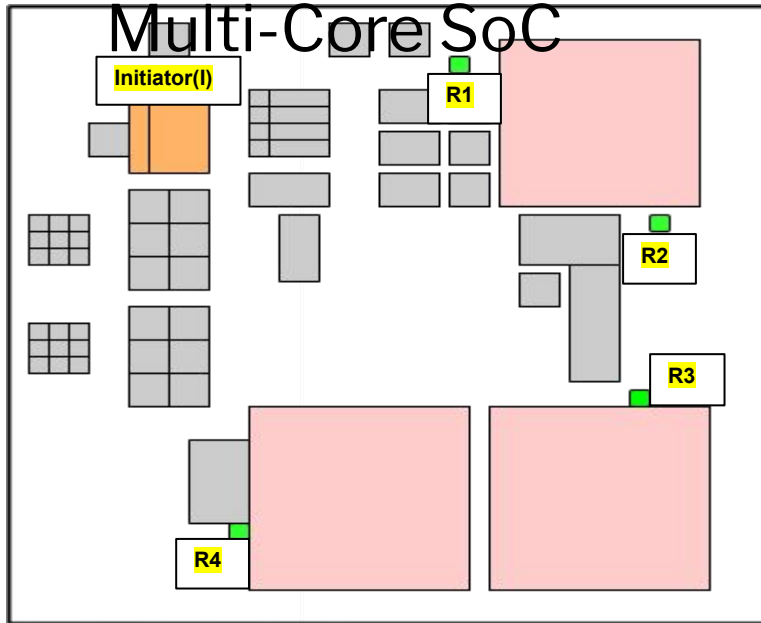
- Metal Lid & Over Mold Flip-Chip package used in ADI SoC (testcase)
- Cadence Voltus for Power/PI analysis
  - Dynamic Power Test VCD peak window
    - High activity test cases for 125°C
  - Scaled, tri-lib (diff temp) and Dynamic vtm output
    - Tile based analysis
- Cadence Celsius for Thermal Analysis
  - 3D/2D model of Enclosure and Metal LID/Over Mold
    - Currently using 2D Model
  - Chip metal stack-up thermal model
  - Laminate, PCB thermal model & Heat Sink model
  - Temperature profile output



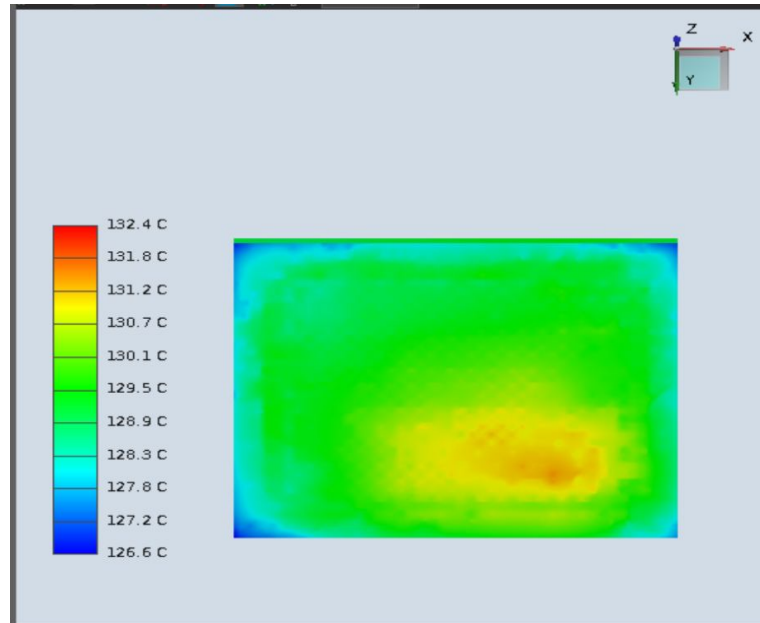
# Silicon data comparison for Chip Thermal Gradient

ADI's

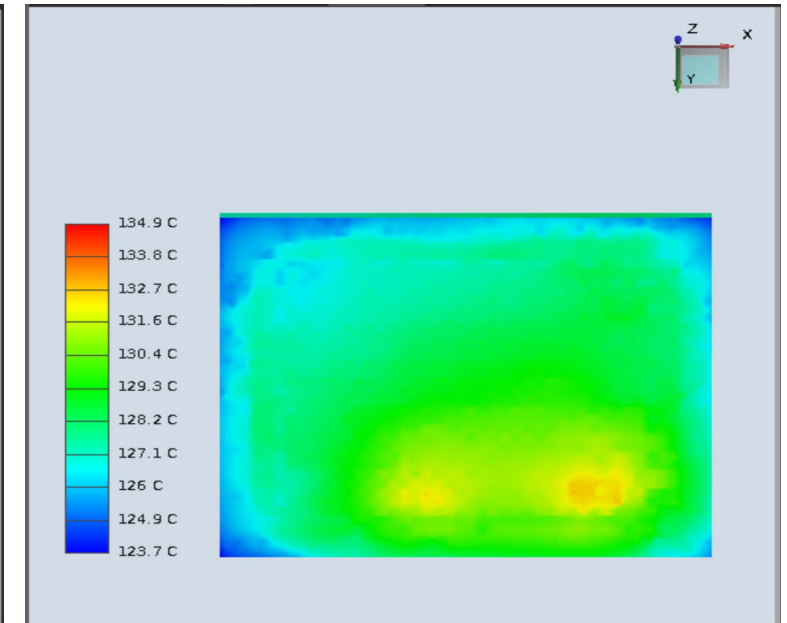
Multi-Core SoC



Test1 : Temperature profile of U1(DIE)



Test2 : Temperature profile of U1(DIE)

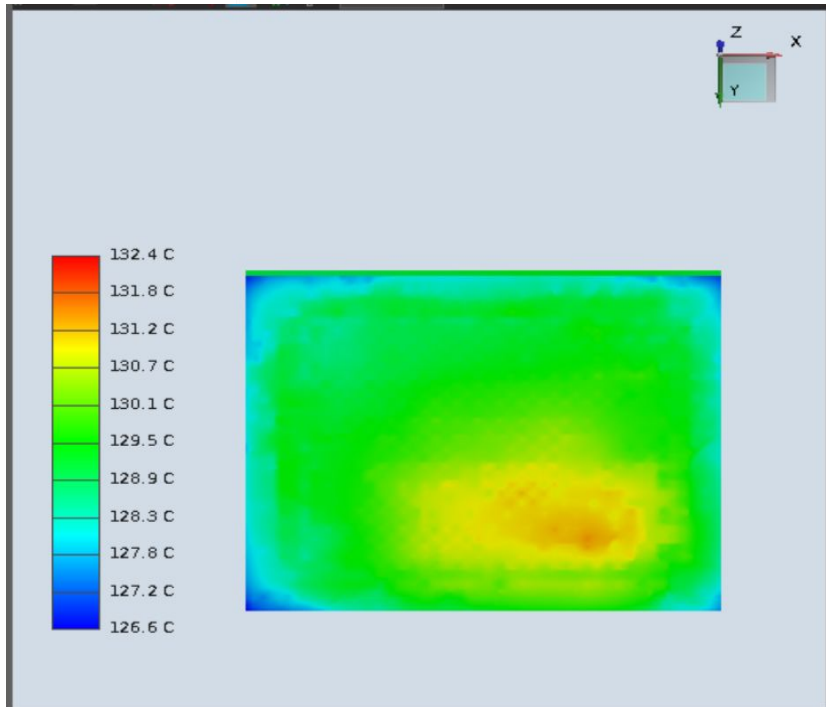


Name	Temp(I)	Temp(R1)	Temp(R2)	Temp(R3)	Temp(R4)	Correlation Difference	Correlation w/o Celsius thermal aware flow
Silicon Data	<b>126.79</b>	<b>127.2</b>	<b>127.46</b>	<b>130.63</b>	<b>126.77</b>		
Celsius Data(Test1)	<b>129.34</b>	<b>129.5</b>	<b>129.90</b>	<b>130.80</b>	<b>129.50</b>	<b>3° C</b>	<b>8° C</b>
Celsius Data(Test2)	<b>127.50</b>	<b>128.1</b>	<b>128.90</b>	<b>130.50</b>	<b>128.70</b>	<b>2° C</b>	<b>8° C</b>

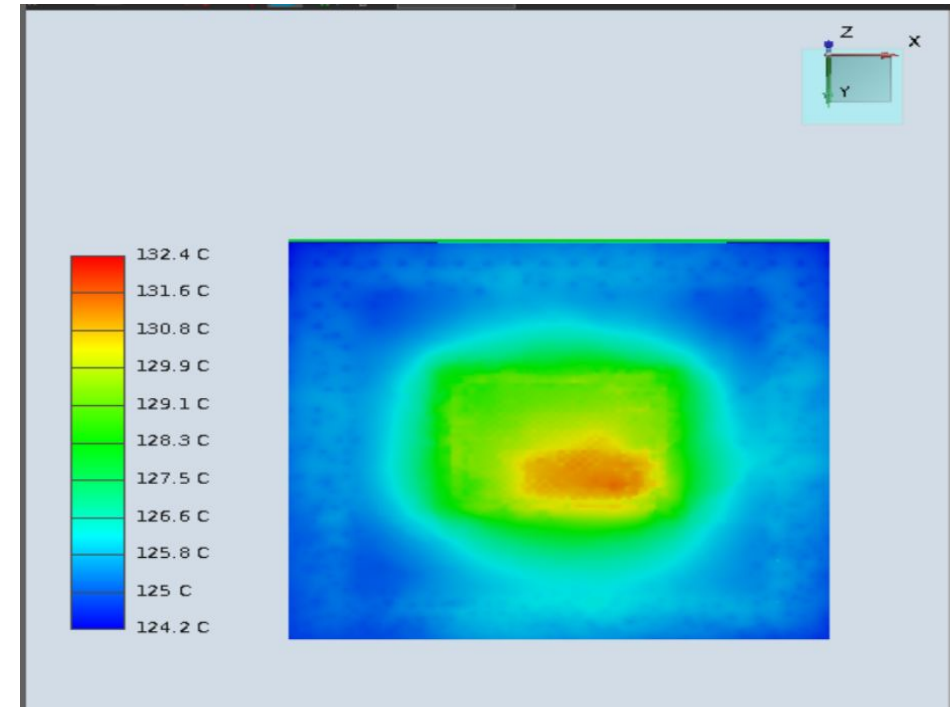


# Temperature profile of U1(DIE)+J1(Package)

**Chip Level View : Temperature profile of DIE for design signoff**



**System View: Temperature profile for optimal probe placement**



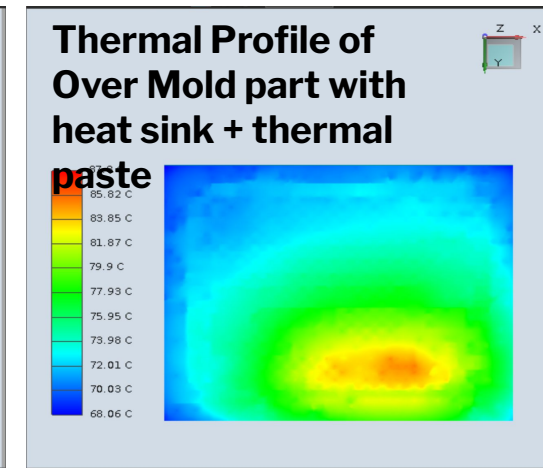
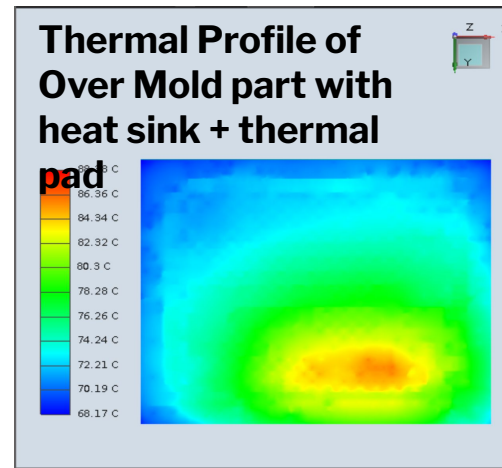
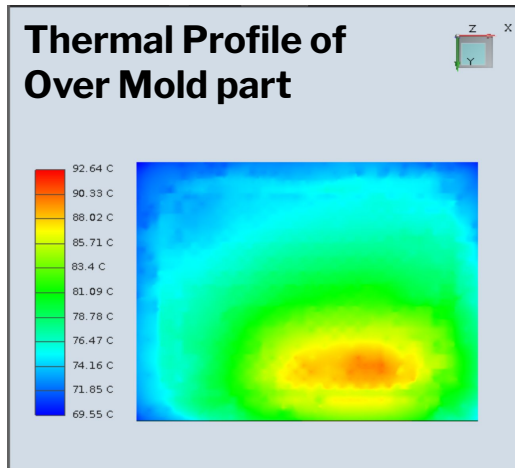
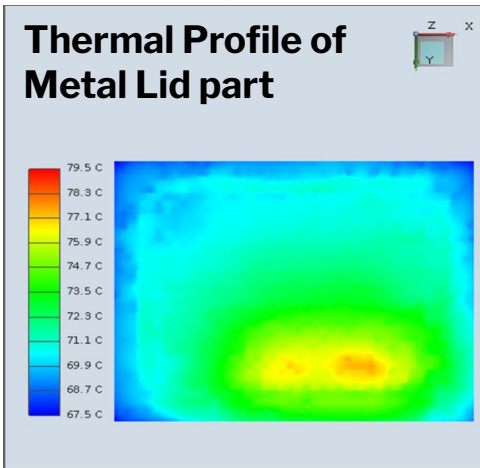
# Thermal Analysis: Metal Lid Vs Over Mold

Ambient Temp	25° C				50° C				70° C				100° C				120° C			
Package	Metal Lid w/o heat sink	Over Mold w/o heat sink	Over Mold with heat sink with thermal paste	Over Mold with heat sink with thermal pad	Metal Lid w/o heat sink	Over Mold w/o heat sink	Over Mold with heat sink with thermal paste	Over Mold with heat sink with thermal pad	Metal Lid w/o heat sink	Over Mold w/o heat sink	Over Mold with heat sink with thermal paste	Over Mold with heat sink with thermal pad	Metal Lid w/o heat sink	Over Mold w/o heat sink	Over Mold with heat sink with thermal paste	Over Mold with heat sink with thermal pad	Metal Lid w/o heat sink	Over Mold w/o heat sink	Over Mold with heat sink with thermal paste	Over Mold with heat sink with thermal pad
Temp(I)	NA	48.97° C	46.4° C	46.7° C	72.01° C	75.1° C	72.2° C	72.5° C	NA	98.5° C	94.8° C	95.2° C	NA	131.8° C	128.4° C	128.8° C	NA	151.9° C	148.5° C	148.9° C
Temp(R1)	NA	49.9° C	47.1° C	47.5° C	71.3° C	76.03° C	72.9° C	73.3° C	NA	99.51° C	95.6° C	96.04° C	NA	132.8° C	129.2° C	129.6° C	NA	152.9° C	149.3° C	149.7° C
Temp(R2)	NA	52.1° C	48.8° C	49.2° C	71.8° C	78.23° C	74.7° C	75.1° C	NA	101.8° C	97.3° C	97.8° C	NA	134.9° C	130.8° C	131.3° C	NA	155° C	150.9° C	151.4° C
Temp(R3)	NA	57.7° C	53.7° C	54.2° C	73.8° C	84.03° C	79.6° C	80.2° C	NA	108.2° C	102.8° C	103.4° C	NA	141.5° C	136.5° C	137.1° C	NA	161.6° C	156.6° C	157.2° C
Temp(R4)	NA	53.1° C	49.8° C	50.2° C	72.1° C	79.3° C	75.7° C	76.1° C	NA	102.9° C	98.4° C	98.9° C	NA	136.2° C	132° C	132.5° C	NA	156.4° C	152.1° C	152.6° C
Thottest(Tj)	NA	66.09° C	61.71° C	62.26° C	79.5° C	92.64° C	87.8° C	88.38° C	NA	117.4° C	111.5° C	112.2° C	NA	151° C	145.6° C	146.3° C	NA	171.1° C	165.7° C	166.4° C
Tj-R3	NA	8.39° C	8.01° C	8.06° C	5.7° C	8.61° C	8.2° C	8.18° C	NA	9.2° C	8.7° C	8.8° C	NA	9.5° C	9.1° C	9.2° C	NA	9.5° C	9.1° C	9.2° C

- The probe placement can be optimized at room temperature.
- The deltaT variation of on-die temperature is a function of application
- Over Mold parts are hotter compared to metal lid parts
  - What kind of thermal solution(ex- heat sink) required can be decided during early design cycle



# Thermal Analysis: Metal Lid Vs Over Mold



Name	Ambient Temp	Temp(I)	Temp(R1)	Temp(R2)	Temp(R3)	Temp(R4)	Thotttest	Thotttest-Max(All the Sensors R3)
Celsius Data for Metal Lid w/o heat sink	50° C	72.01° C	71.3° C	71.8° C	73.8° C	72.1° C	79.5° C	5.7° C
Celsius Data for Over Mold w/o heat sink	50° C	75.1° C	76.03° C	78.23° C	84.03° C	79.3° C	92.64° C	8.61° C
Celsius Data for Over Mold with heat sink with thermal pad	50° C	72.5° C	73.3° C	75.1° C	80.2° C	76.1° C	88.38° C	8.18° C
Celsius Data with heat sink with thermal paste	50° C	72.2° C	72.9° C	74.7° C	79.6° C	75.7° C	87.8° C	8.2° C

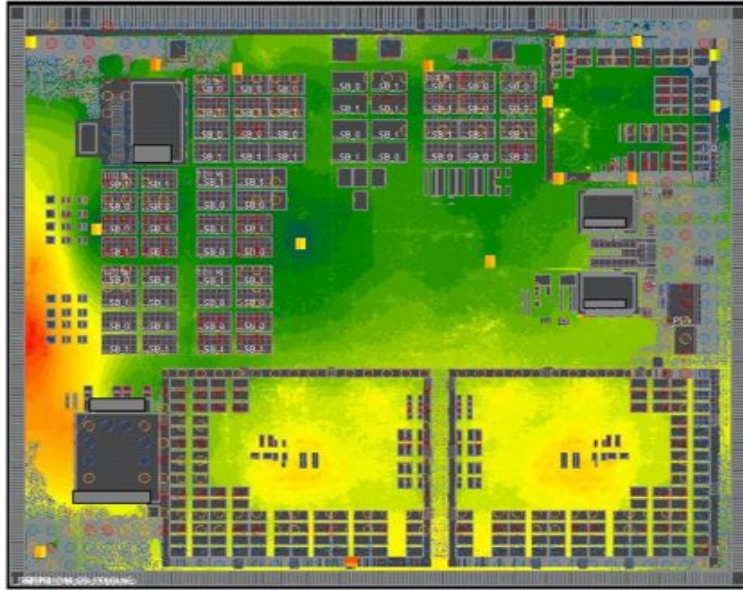
- The probe placement can be optimized at room temperature.
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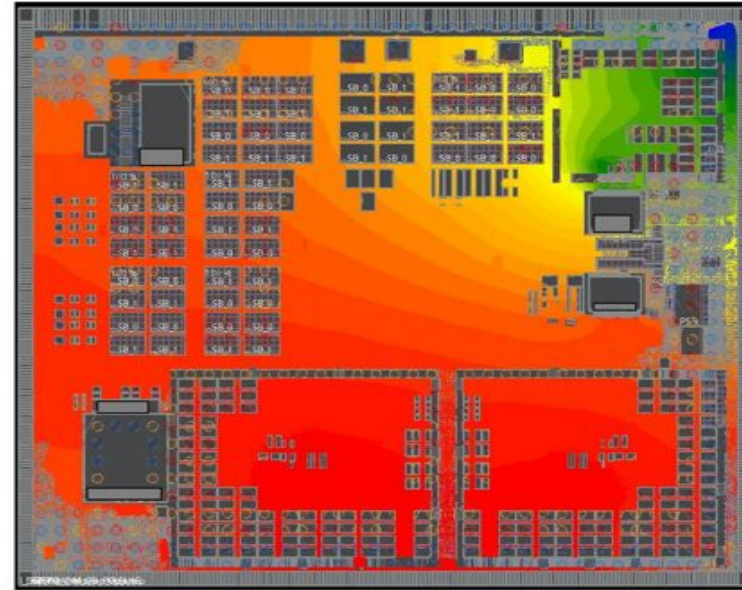
# EM Violation due to thermal impact

Rail Analysis Results with Package and Die



No EM  
Violation

Thermal Aware Rail Analysis Results with Package and Die



More EM  
Violation

- Thermal Analysis generated Thermal Chip Gradient adds impact over Die EM Violation.
- EM violation increased With Thermal Aware Rail Analysis.
- It helped the designer to improve the thermal margin for die.



# Conclusion

- Successfully showcased effectiveness of Thermal-aware electrical analysis flow
  - Automated and tightly integrated Power Integrity (DC-IR/EM) and Thermal Analysis solution enabled chip designer in electrical and thermal sign-off
  - Enabled ADI customers to reduce cost with effective Thermal Gradient, less heat sink use, and improve the reliability
  - Identified issues using Thermal Aware electrical Analysis flow that escaped traditional analysis.
  - Improved EM sign-off flow
- Chip thermal gradient used for electrical analysis is 2°C to 3°C (3%) of silicon data
  - Good correlation between Cadence Celsius and Silicon data
  - Accuracy can be improved with optimal sensor placement

## Future Work

- System level validation of electro-thermal analysis results
- SiP with different packages and integrated Board Model
- SoC's without Thermal Monitor
- Optimal location for Thermal Sensors



# Acknowledgements

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Thank you!

Questions?

